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RTC-BUF Overview

Unless you are interfacing with other digital equipment, input and output levels may not be the standard zero and +5 volts. It is often necessary to monitor voltages of greater than 5 volts and less than zero. In a like manner, controlling external components frequently requires more than 5 volts TTL has to offer. The 24 input lines of the RTC-BUFIO board can withstand inputs of +/-30 volts. The 24 output lines are open-collector, capable of switching 50v at 250ma. On the other hand, the RTC-BUF50 is designed for interfacing directly with the IDI-24 (24 opto-isolated inputs), the IDO-24 (24 relay contact outputs), or the industry standard rack mounts for AC/DC I/O modules.

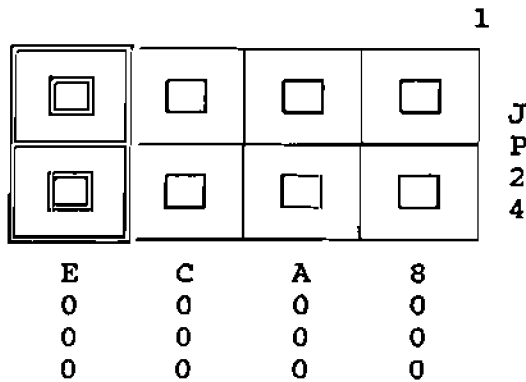
Like its expansion I/O predecessors, the RTC-BUF boards requires an 8k block of I/O space, but multiple I/O boards can all share the same 8k block. Each 8k block is divided into 16 function selects. The RTC-BUFIO board decodes 8 of these selects. Each 8255 requires one select. This means four RTC-BUF boards can co-exist within the same 8k block.

Input and output connections are made through square pin headers which accept a standard ribbon cable connection. Optional screw termination adapters can be used to attach to each of the RTC-BUFIO ports via ribbon cable.

Address Selection

The I/O address space is broken down by the processor board into 8k blocks. These blocks are 8000H-9FFFH, 0A000H-0BFFFH, 0C000H-0DFFFH, and 0E000H-0FFFFH. The expansion board can select one of the 8k blocks through a jumper on JP24.

Base Address Selection JP24

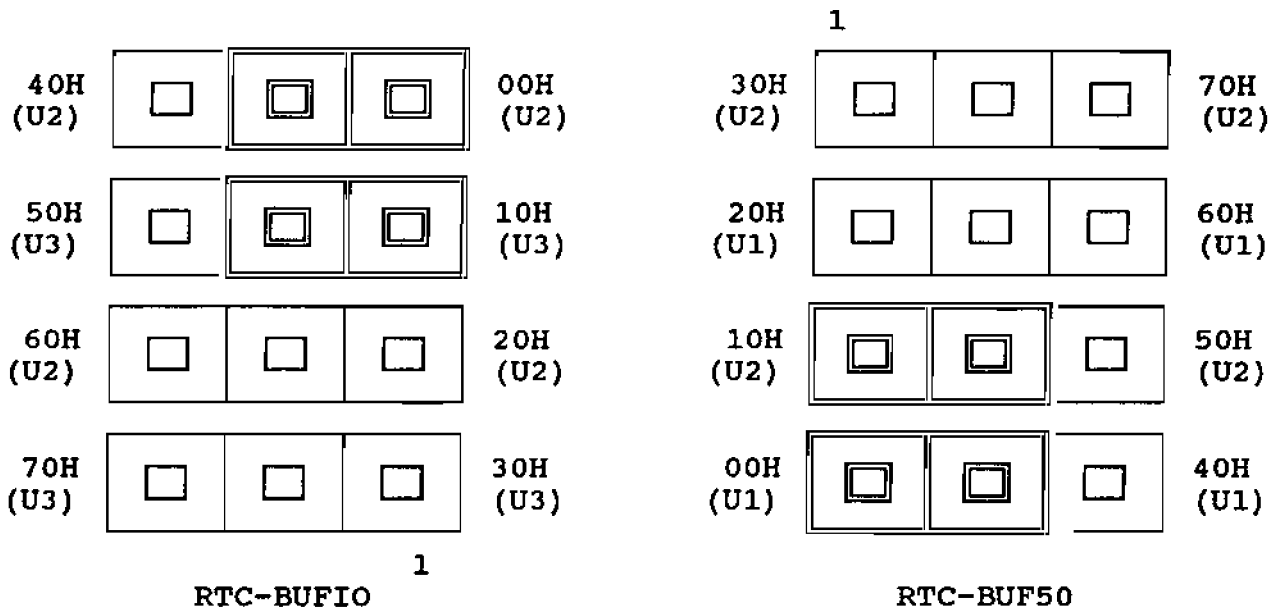


This example shows the Base Address of 0E000H Enabled

RTC-BUF

The 8k address block selected from JP24 is broken down by the RTC-BUF boards into 8 function selects. Since the RTC-BUF boards use only two of the 8 available selects, multiple boards can be used within the same 8k address block. Four possible selects are available for addressing each 8255.

Offset Address JP19



This example shows the Offset Address of 00H enabled for the first 8255 and 10H enabled for the second. When the Base selection from JP24 is added to the Offset selections from JP19, the actual address is 0E000H for the first 8255 and 0E010H for the second.

On the RTC-BUF10, input and output, is handled through its own 8255 Programmable Peripheral Interface. Each PPI has 24 bits of programable I/O. The interface hardware on the RTC-BUF10 requires that 8255-U2 be configured as 24 input lines and 8255-U3 be configured as 24 output lines.

On the RTC-BUF50, each 8255 can be either input or output. This setup will be determined by your choice of interface cards. The 8255s may be configured as both inputs, both outputs, or one of each.

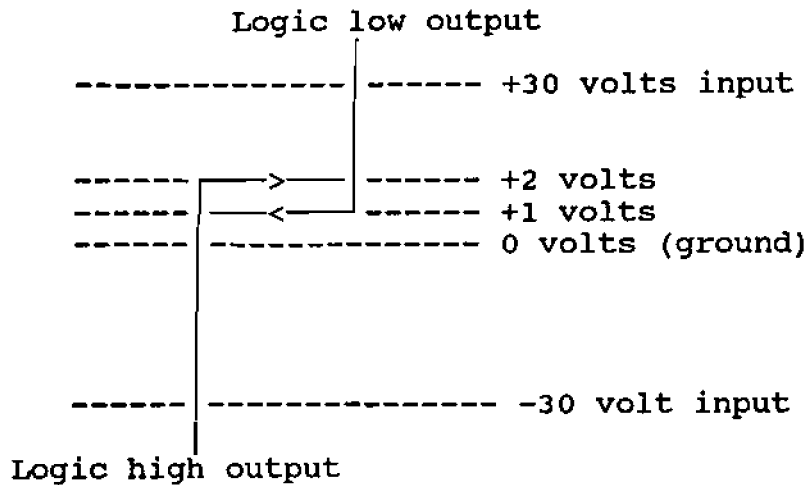
The 8255 contains four registers (or ports). The first three are I/O registers, one for each of Port A, Port B, and Port C. The fourth register (mode port) is used to program the first three 8-bit ports individually as input or output. When reset or at power-up, the PPI's three ports are automatically set as all inputs. Writing a value of 9BH to the mode port will also set all the ports as input, whereas writing a value of 80H to the mode port will set all ports as outputs.

The ports are accessed by writing to the Base address (JP24) plus Offset address (JP19) plus:

0H for Port A	(0E000H + x0H + 0H = 0E0x0H)
1H for Port B	(0E000H + x0H + 1H = 0E0x1H)
2H for Port C	(0E000H + x0H + 2H = 0E0x2H)
3H for the Mode Port	(0E000H + x0H + 3H = 0E0x3H)

Input Connections
RTC-BUFIO

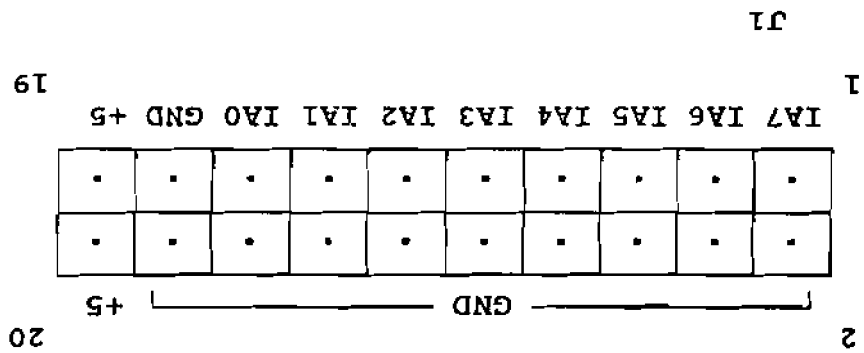
The RTC-BUFIO board uses 1489s as input inverter/level shifters. The 1489 input inverters will manage inputs levels as high as +/- 30 volts. The inverter output will switch to a high logic level when the input signal drops from above +2 volts down to below +1. The TTL output switches to a logic low level when the input rises (from below +1 volt) above the +2 volt level. This hysteresis gives about 1 volt of noise immunity. All inputs have a 2-7k input impedance.



U1, the input PPI, receives all 24 input bits through its Port's A, B, and C. Inputs on J1 are accessed through Port A, J2 inputs through Port B, and J3 inputs through Port C. The input connectors are 2-by-10 right-angle square-pin headers. Every input has a complimentary ground pin. Four additional pins contain an extra pair of grounds and a pair internal 5 volt outputs. Caution, internal 5 volts is not provided to power additional equipment, but merely to provide a handy pull-up source.

9/15/92

This is typical for all three inputs J1, J2, and J3

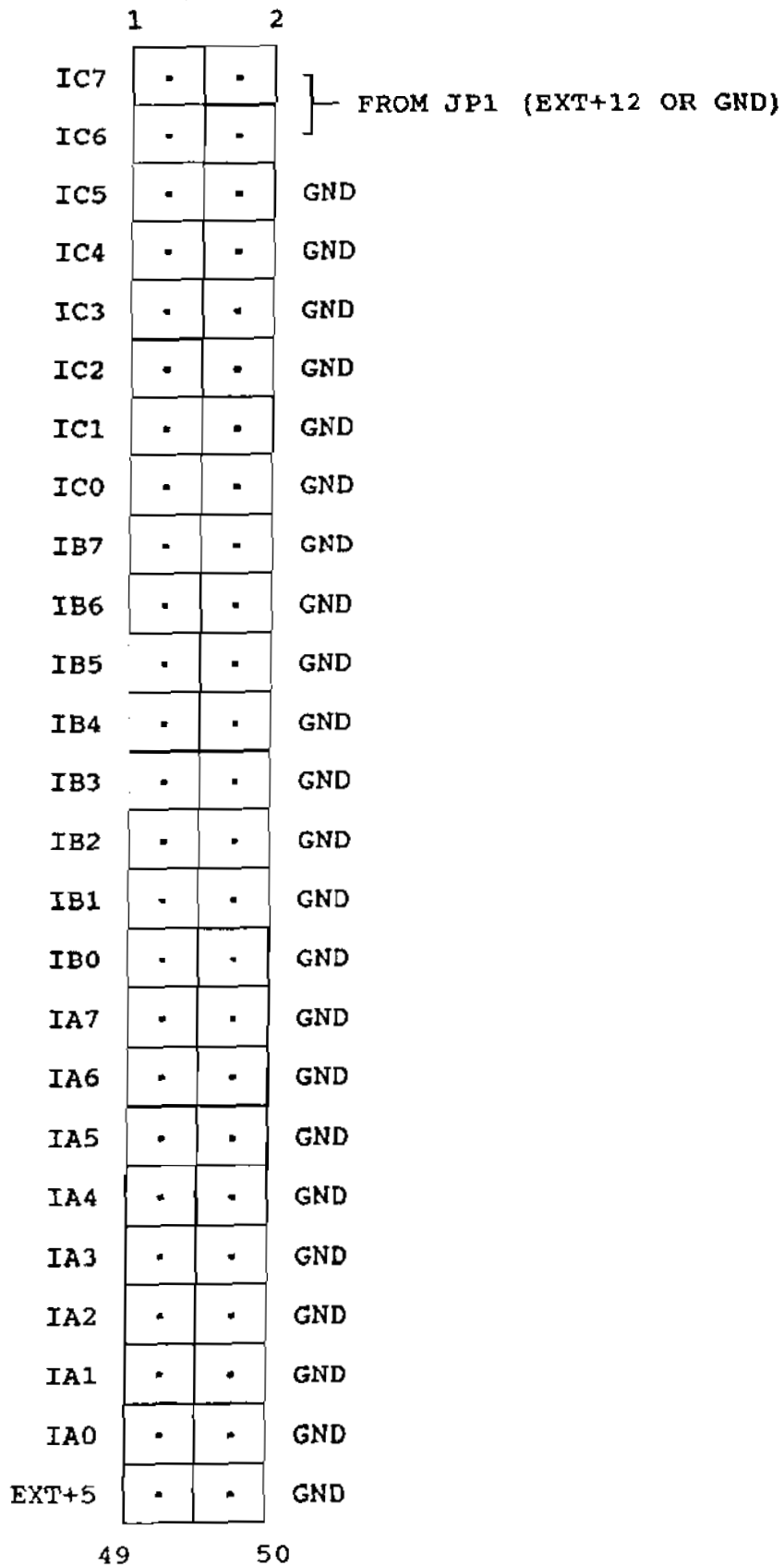


RTC-BUFIO Inputs

Input Connections
RTC-BUF50

Each 8255 on the RTC-BUF50 has 24 TTL inputs ,if so configured through the mode port. Only logic levels, +5 volts and ground, are allowed. All three 8-bit ports are available through a single 2-by-25 square-pin header. The RTC-BUF50 has two such connectors, one for each 8255.

RTC-BUF50 as an INPUT PORT



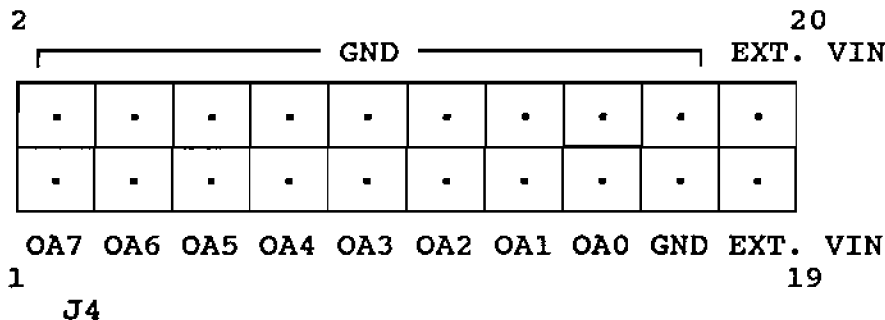
49 50

Output Connections
RTC-BUFIO

The RTC-BUFIO uses Sprague open-collector drivers which invert latched TTL data from the output PPI. Each of the three 8-bit devices can support its own external voltage source up to 50 volts. Each driver can handle loads of 125 mA maximum all drivers ON or 500 mA one driver ON (100% duty cycle @ +50 degrees C, higher temperatures will determine derating specifications).

U3, the output 8255, is configured as all inputs upon reset or power-up. The user must assign the mode port the value 80H to reconfigure it as all outputs. Pull-downs are placed on the inputs of the ULN2803's drivers to hold the outputs off until the mode of the PPI can be set to all outputs and take control of all 24 drivers through its Port's A, B, and C. Port A outputs are accessed through J4, Port B outputs through J5, and Port C outputs through J6. The output connectors are 2-by-10 right-angle square-pin headers. Every output has a complimentary ground pin. Four additional pins contain an extra pair of grounds and a pair of external voltage inputs. If external voltages are not used, the internal 5 volt supply can be enabled. Caution, internal 5 volts is not provided to power additional equipment, but merely to provide a handy pull-up source.

RTC-BUFIO Outputs



This is typical for all three outputs J4, J5, and J6.

When not using external voltages on the output connectors, the 5 volt system supply can be enabled as an external pull-up source. Each output port has an internal 5 volt supply header, JP1 for J4, JP2 for J5, and JP3 for J6. A piece of bus wire must be soldered across the pads to enable the internal 5 volt system supply.



JP1 is shown with a piece of wire soldered across the pads of JP1, enabling the internal 5 volt system supply to be used as the J4 open-collector source voltage.

Output Connections
RTC-BUF50

Each 8255 on the RTC-BUF50 has 24 TTL outputs ,if so configured through the mode port. Only logic levels, +5 volts and ground, are created. All three 8-bit ports are available through a single 2-by-25 square-pin header. The RTC-BUF50 has two such connectors, one for each 8255.

RTC-BUF50 as an OUTPUT PORT

	1	2	
OC7	.	.	} FROM JP1 (EXT+12 OR GND)
OC6	.	.	
OC5	.	.	GND
OC4	.	.	GND
OC3	.	.	GND
OC2	.	.	GND
OC1	.	.	GND
OC0	.	.	GND
OB7	.	.	GND
OB6	.	.	GND
OB5	.	.	GND
OB4	.	.	GND
OB3	.	.	GND
OB2	.	.	GND
OB1	.	.	GND
OB0	.	.	GND
OA7	.	.	GND
OA6	.	.	GND
OA5	.	.	GND
OA4	.	.	GND
OA3	.	.	GND
OA2	.	.	GND
OA1	.	.	GND
OA0	.	.	GND
EXT+5	.	.	GND
	49	50	

DEMO Program for the RTC-BUFIO and RTC52 (BASIC-52)

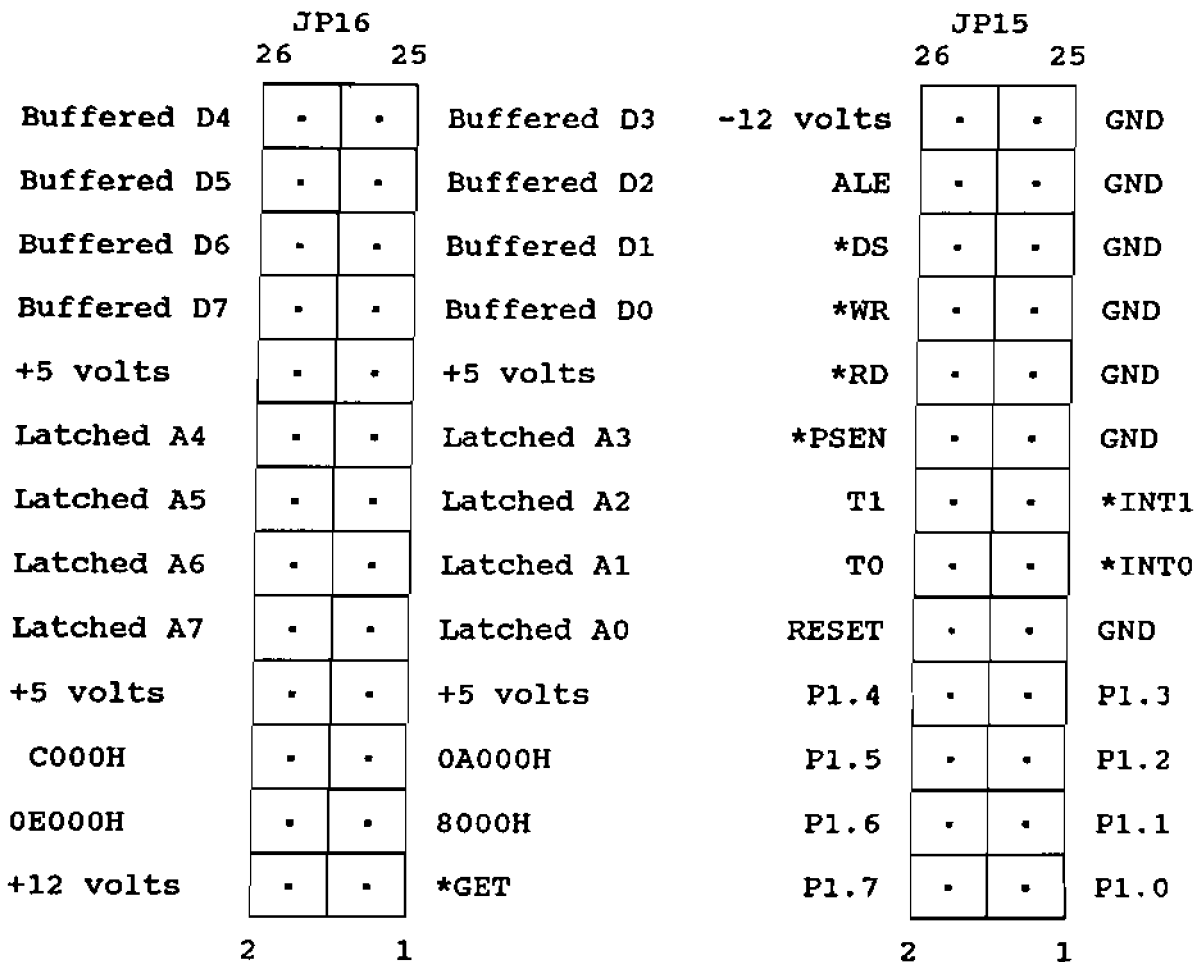
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10 INPUT "What is the RTC-BUFIO Base Address (0E000H)?"B
20 INPUT "What is the PPI's Inputs Offset Address (00H)?"IO
30 INPUT "What is the PPI's Outputs Offset Address (10H)?"OO
40 I=B+IO : REM Input PPI's Address
50 O=B+OO : REM Output PPI's Address
60 XBY(I+3)=9BH : REM Default on power-up IS 9BH,
70 REM all inputs, this is just for show
80 XBY(O+3)=80H : REM Must set this to all outputs with 80H
90 PRINT "Menu Selection"
100 PRINT
110 PRINT "1 = Read and display input values"
120 PRINT "2 = Write a value to output Port A"
130 PRINT "3 = Write a value to output Port B"
140 PRINT "4 = Write a value to output Port C"
150 PRINT "5 = Loop writing each output port with the value"
160 PRINT "read from the corresponding input port"
170 PRINT "0 = End"
180 G=GET : REM Dummy GET
190 G=GET : IF G=0 THEN 190 : REM Try again if no keys
200 IF (G<30H).OR.(G>35H) THEN 190 : REM Try again if illegal
210 ON G-30H GOTO 220,240,320,360,400,440
220 REM *****
230 END ; REM That's all folks!
240 REM *****
250 REM Read the input Ports
260 IA=XBY(I)
270 IB=XBY(I+1)
280 IC=XBY(I+2)
290 REM Now display 'em
300 PH0. "Port A =",IA," Port B =",IB," Port C =",IC
310 GOTO 90
320 REM *****
330 INPUT "What is the value to write to Port A",V
340 XBY(O)=V
350 GOTO 90
360 REM *****
370 INPUT "What is the value to write to Port B",V
380 XBY(O+1)=V
390 GOTO 90
400 REM *****
410 INPUT "What is the value to write to Port C",V
420 XBY(O+2)=V
430 GOTO 90
440 REM *****
450 REM Read 'em 'n' Write 'em
460 XBY(O)=XBY(I)
470 XBY(O+1)=XBY(I+1)
480 XBY(O+2)=XBY(I+2)
490 G=GET
500 IF G=0 THEN 440
510 GOTO 90

```

VERTICAL-STACKING I/O EXPANSION

The vertical-stacking connectors pass all the necessary I/O to each expansion board added to the system. The buffered address/data bus (AD0-AD7), the latched address bus (A0-A7), and the upper four decoded 8k address blocks (8000H, A000H, C000H & E000H) are grouped together. Control lines are bundled separately on a separate vertical connector. These two connectors alone provide adequate mechanical stability for the stacking arrangement, but corner mounting holes are provided for #4 x 9/16" spacers.

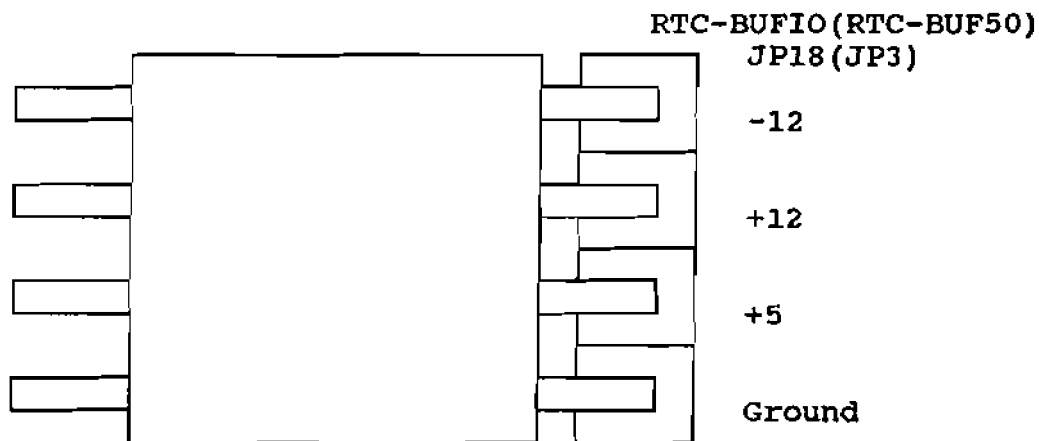
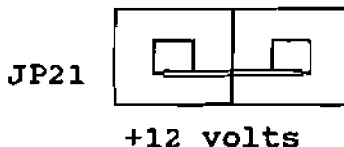
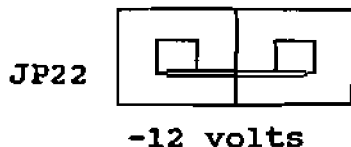


System Power

Power is connected to the RTC system through any of the expansion boards. Each four pin Molex style connector can provide ground, +5, +12, and -12 volts to the whole system. Most system boards require 5 volts only. The RTC-BUFIO board requires only +5 volts. Some boards require +12, -12, or both but have on board DC/DC converters to produce any voltages necessary from 5 volts.

The 4-pin molex connector (JP18 on the RTC-BUFIO and J3 on the RTCBUF50) will supply +5 volt power to the whole RTC system, jumpers added in JP21 and JP22 will connect the +/-12 volts of power connector to the vertical expansion headers (and the other expansion boards). This is generally not necessary and is provided only as a convenience to the user.

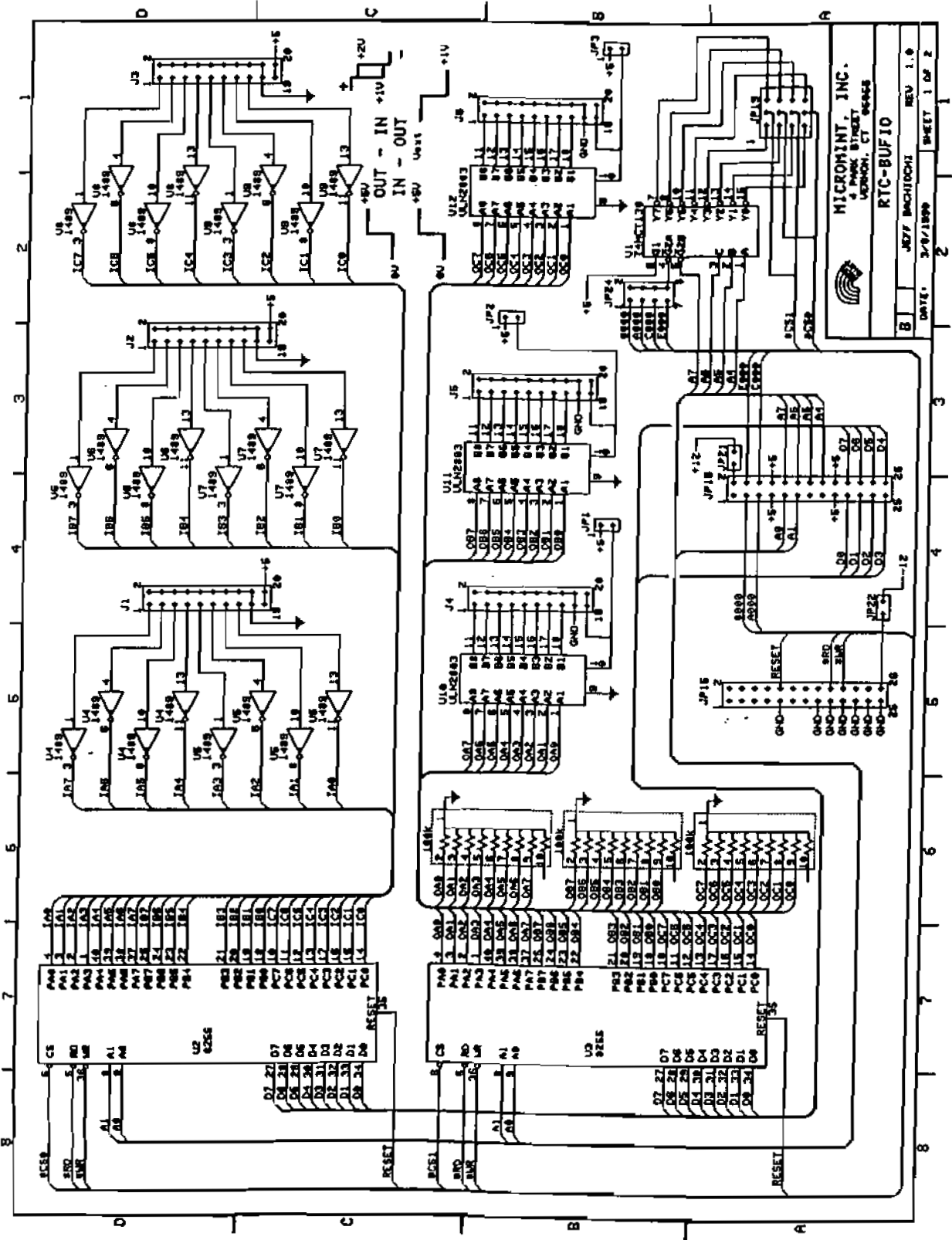
In addition the RTC-BUF50 can route on-board power through the 50-pin ribbon cable by adding JP3 and JP4. This is meant to supply external voltage for the IDI-24 and IDO-24 when the system is small and the supply can handle the current. It is recommended that a separate external supply be used with all IDI-24 and IDO-24 systems.



Power requirements for the RTC-BUF boards are as follows:

- RTC-BUFIO = 5 volts @ 120ma (no additional external loads)
- RTC-BUF50 = 5 volts @ 50ma (no additional external loads)

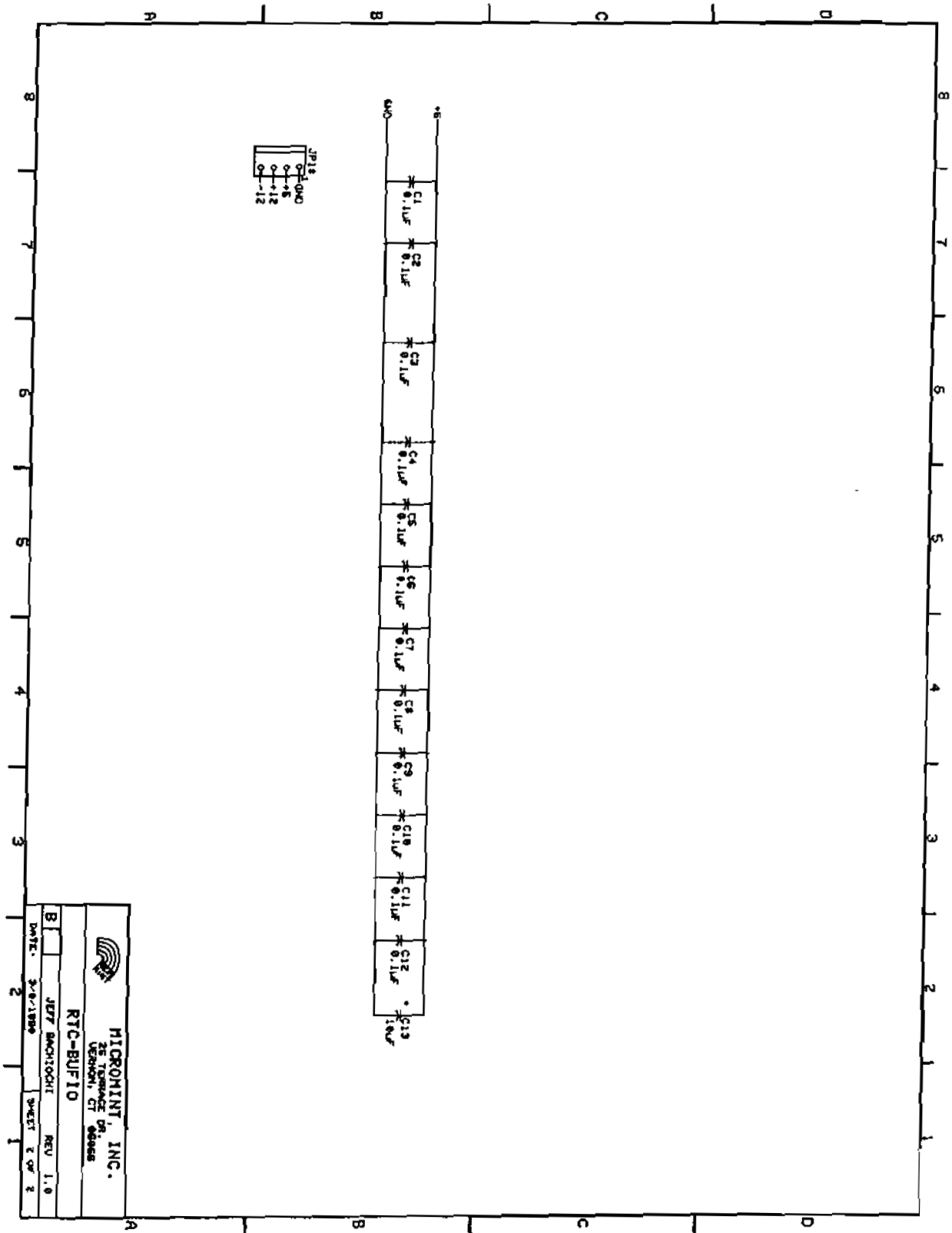
RTC-BUFIO SCHEMATICS (1 of 2)



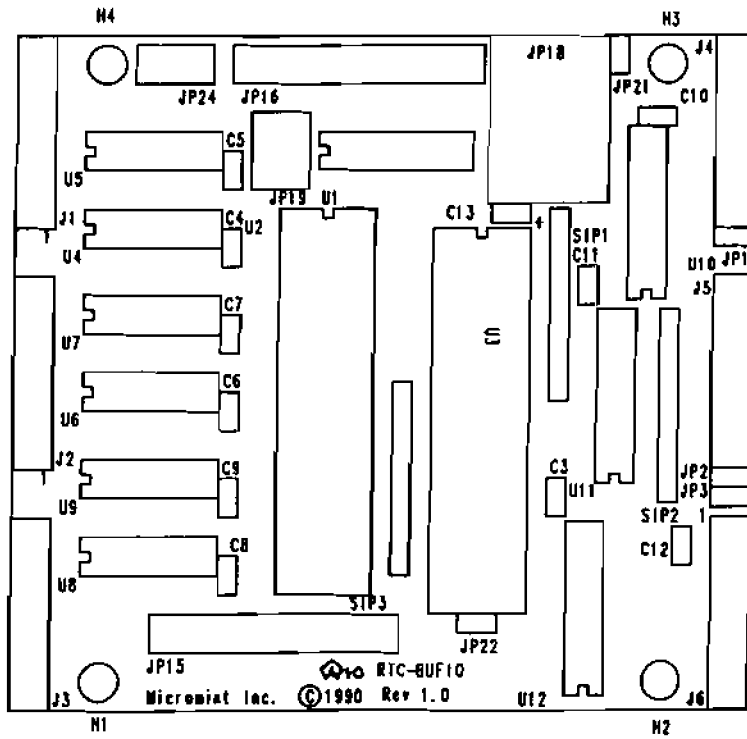
MICROMINT, INC.
 1000 STREET
 WASHINGTON, CT 06095

RTC-BUFIO

DATE: 3/8/1999 SHEET 1 OF 2



RTC-BUFIO SCHEMATICS (2 of 2)



Silkscreen for the RTC-BUFIO

PARTS LIST for the RTC-BUFIO

DESIGNATION	PART#	DESCRIPTION
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Printed Circuit Board

PCB1		RTC-BUFIO Printed Circuit Board
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Integrated Circuits

U1	74HCT138	3-to-8 Decoder
U2, U3	8255	Programable Peripheral Interface
U4 - U9	1489	Quad Level Shifter
U10 - U12	ULN2803A	Octal Open-collector Driver

Resistors

SIP1 - SIP3	100k	9-resistor SIP, one side common
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Capacitors

C4 - C12	0.1 μ F	Monolithic
C13	10 μ F	Tantalum

Connectors

J1 - J6	2x10	Right-Angle Square-Pin Header
JP15, JP16	2x13	Vertical-Stacking Header
JP18	1x4	Right-Angle Molex Header
JP19	3x4	Square-Pin Header
JP25	2x4	Square-Pin Header

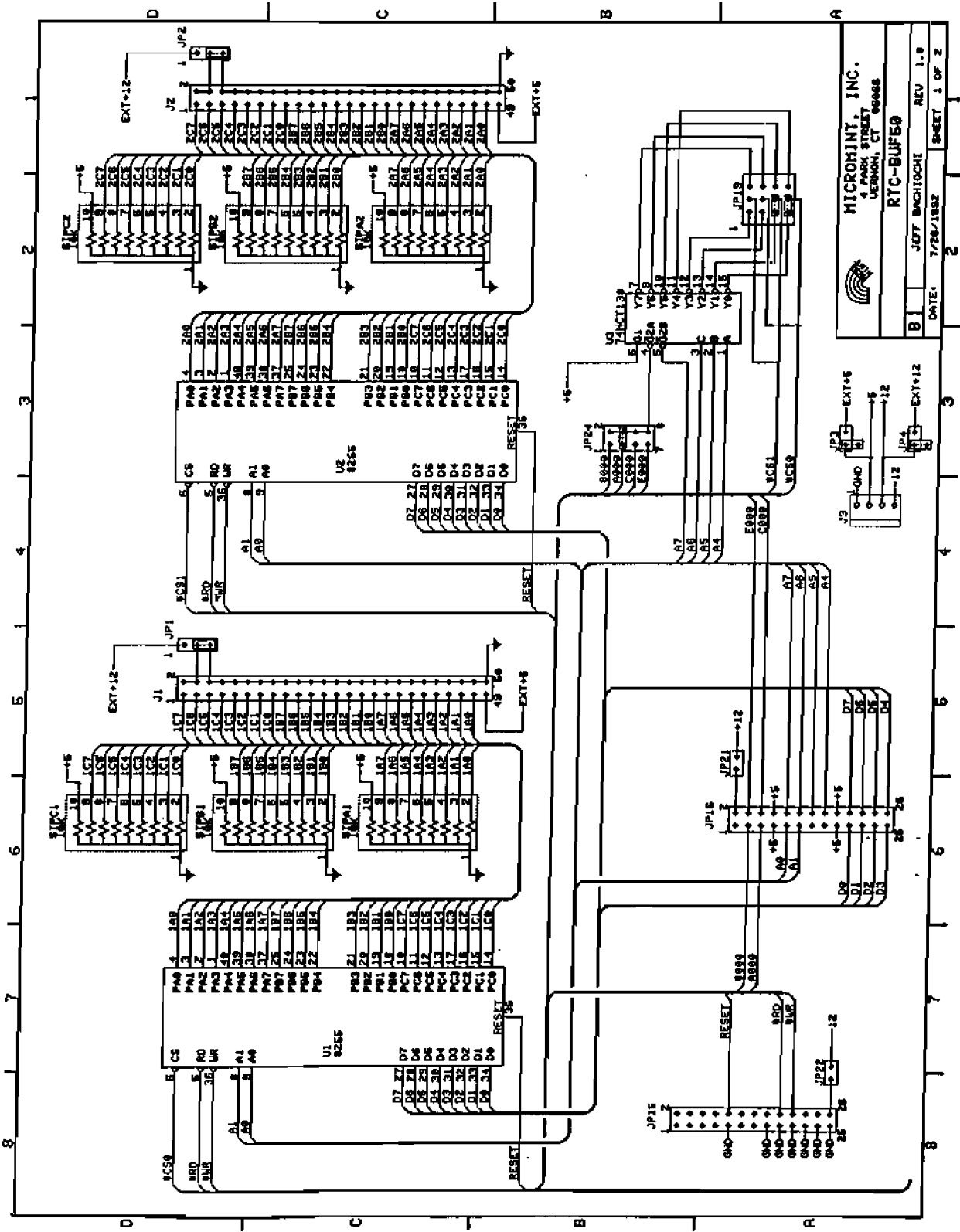
Sockets

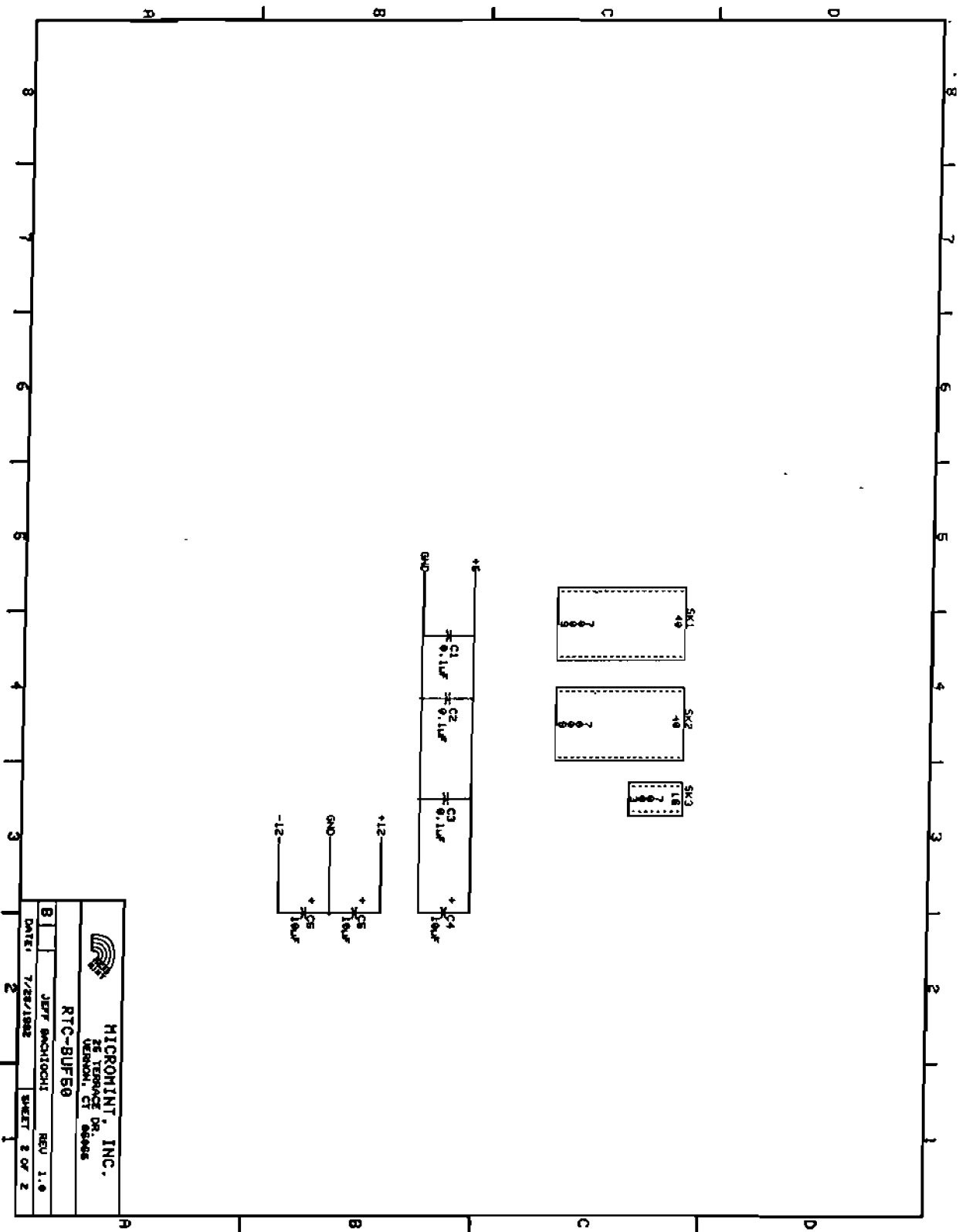
SK1	16 Pin	IC Socket
SK2, SK3	40 Pin	IC Socket
SK4 - SK9	14 Pin	IC Socket
SK10 - SK12	18 Pin	IC Socket

Miscellaneous

SJ1 -SJ3		Shorting Jumper
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RTC-BUF50 SCHEMATICS (1 of 2)

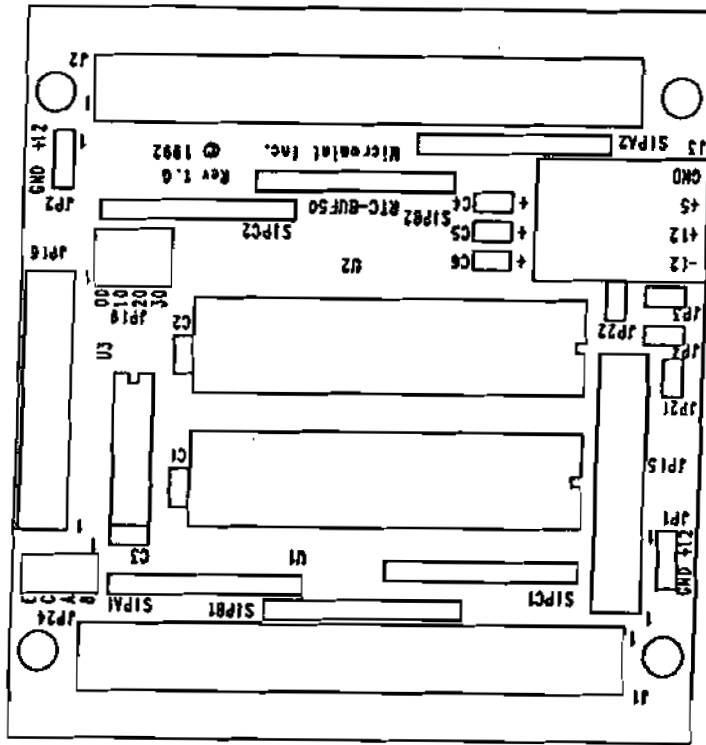




RTC-BUF50 SCHEMATICS (2 of 2)

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Silkscreen for the RTC-BUF50



PARTS LIST for the RTC-BUF50

DESIGNATION	PART#	DESCRIPTION
<u>Printed Circuit Board</u>		
PCB1		RTC-BUF50 Printed Circuit Board
<u>Integrated Circuits</u>		
U3	74HCT138	3-to-8 Decoder
U1, U2	8255	Programable Peripheral Interface
<u>Resistors</u>		
SIPA1 - SIPB3	10k	9-resistor SIP, one side common
<u>Capacitors</u>		
C1 - C3	0.1 μ F	Monolithic
C4 - C6	10 μ F	Tantalum
<u>Connectors</u>		
J1 - J2	2x25	Square-Pin Header
J3	1x4	Right-Angle Molex Header
JP1 - JP2	1x3	Square-Pin Header
JP3 - JP4	1x2	Square-Pin Header
JP15, JP16	2x13	Vertical-Stacking Header
JP19	3x4	Square-Pin Header
JP21 - JP22	1x2	(pads only)
JP25	2x4	Square-Pin Header
<u>Sockets</u>		
SK3	16 Pin	IC Socket
SK1, SK2	40 Pin	IC Socket
<u>Miscellaneous</u>		
SJ1 -SJ7		Shorting Jumper